REMARKS

This amendment responds to the Office Action mailed on August 26, 2004. Filed concurrently herewith is a *Request for a Three Month Extension of Time* which extends the shortened statutory period for response to expire on February 28, 2005. Accordingly, Applicants respectfully submit that this response is being timely filed.

Claims 1-11 were pending. In the Office Action mailed August 26, 2004, amendments to the specification, drawings and claims were either suggested or required. Applicants have so amended the specification, drawings and claims. New claims 12-20 are submitted for examination on their merits. Accordingly, claims 1-20 are now pending in the present application, and Applicant believes these claims are in proper condition for allowance for the reasons set forth below.

Priority

In accordance with the suggestions in paragraph 1 of the Office Action, the specification has been amended above to reference that the present application is a continuation of pending PCT Application No. PCT/GB99/03168, filed October 11, 1999, which is incorporated by reference in its entirety herein, and claims priority to U.S. Provisional Patent Application No. 60/115,952 filed on January 14, 1999, now abandoned, which is incorporated by reference in its entirety herein, and claims priority to GB Patent Application No. 9822075.9, filed October 10, 1998, now abandoned, which is incorporated by reference in its entirety herein. A copy of the certified priority document for (GB) 9822075.9 is also submitted herewith.

It should be noted that the present application claims priority to GB Patent Application No. 9822075.9 filed October 10, 1998. Further, the present application is the U.S. national stage application of PCT Application No. PCT/GB99/03168. When filing the present application, Applicants inadvertently indicated on the transmittal page filed with the present application that it was a continuation-in-part of PCT/GB99/03168. However, the present application is actually a continuation of PCT Application No. PCT/GB99/03168 as its U.S. national stage application. Thus, the effective priority date of the present application is the October 10, 1998 filing date of GB Patent Application No. 9822075.9. As can be seen from the copy of the certified priority document for GB Patent Application No. 9822075.9 submitted concurrently herewith, the

disclosure in the specification of the present application is identical to and fully supported by GB Patent Application No. 9822075.9. Hence, the present application has an effective priority date of October 10, 1998.

Drawings

Paragraph 4 of the Office Action objected to the drawings as failing to comply with 37 CFR 1.84(p)(4). With respect to the objections to FIGS. 1-6, Applicants have submitted herewith Replacement Sheets for Figs 5-7 to the drawings to eliminate the use of the numerals 1, 2 and 3 to designate intermediate representation blocks in Figures 6 and 7. In particular, the numerals 100, 200 and 300 have been respectively substituted for 1, 2 and 3 in Fig. 6. In Fig. 7, the numerals 100, 200a, 200b and 300 have been respectively substituted for the numerals 1, 2a, 2b and 3. The specification has been amended accordingly to reflect these changes to the reference numerals.

Paragraph 5 of the Office Action object to the drawings as failing to comply with 37 CFR 1.84(p)(5). Initially, it is asserted in the Office Action that characters 1-12 in FIGS. 1-5 are not mentioned in the description. It is clearly described on page 18, lines 21-25 of the specification of the present application that FIGS. 1-5 show the step by step progression of how the intermediate representation is generated. Reference numerals 1-12 indicate the incremental progression of the steps in generating the intermediate representation, where each of the 12 steps in the illustrative example are identified by the reference numerals 1-12 appearing in FIGS. 1-5. These steps are further clearly described in the following pages 19-21 of the specification. By the above amendment, Applicants have amended the specification to make clear reference to numerals 1-12 appearing in the figures, and it is respectfully submitted that such changes do not add any new subject matter to the present application.

Paragraph 5 of the Office Action further indicates that the 'expression forest' described in the specification is not labeled in any of FIGS. 1 to 5. Applicants note that FIGS. 1 to 5 together illustrate the 'expression forest,' as described on page 15, 8th paragraph of the specification. All of the expression trees referenced by each of the register objects together form the 'expression forest,' as described on page 3, lines 19-21 of the specification. Thus, it can be seen that the 'expression forest' changes as more expression trees are generated in the progression through

FIGS. 1 to 5. Thus, FIGS. 1 to 5 as a whole are the expression forest and this is clearly referenced and described in the specification. Reconsideration is respectfully requested.

Provisional Double-Patenting Rejections

Paragraphs 8 and 9 of the Office Action provisionally rejected claims 1-11 under 35 U.S.C. § 101 as claiming the same subject matter of that of claims 1-11 of co-pending Applications Nos. 10/165,012 and 10/165,029. Applicants respectfully submit that this double patenting rejection is moot since preliminary amendments canceling Claims 1-11 were filed in each of these co-pending applications. Accordingly, Applicants respectfully request withdrawal of the rejection.

Paragraph 10 of the Office Action provisionally rejected claim 1 items (i) and (ii) under 35 U.S.C. § 101 as claiming the same subject matter of that of claim 11 items (i) and (ii) of co-pending U.S. Patent Application No. 09/827,974. Applicants note that in addition to items (i) and (ii), claim 1 of the present invention further recites the limitation that "at least one variable sized register is represented by plural register objects, one register object being provided for each possible size of the variable sized register." Claim 11 of co-pending U.S. Patent Application No. 09/827,974 is directed toward a separate invention and does not recite this feature. Accordingly, claim 1 of the present invention does not recite the same invention as that of claim 11 of co-pending U.S. Patent Application No. 09/827,974 and Applicants respectfully request withdrawal of the rejection.

Claim Rejections Under 35 U.S.C. §103

Paragraph 14 of the Office Action rejects claims 1-4 and 6-11 under U.S.C. § 103(a) as being obvious over Aho et al., "Compiler, principles, techniques, and tools" book, published in 1986 (hereinafter "Aho") in view of U.S. Patent No. 5,613,117 to Davidson. Applicant respectfully traverses this rejection and submits that the claims at issue are patentable over those patents for the following reasons.

CLAIMS 1-11

Claims 1-11 are directed to a method and system for generating an intermediate representation (IR) of program code by generating: i) a plurality of register objects for holding variable values to be generated by the program code and ii) a plurality of expression objects representing fixed values and/or relationships between the fixed values and the variable values according the program code. According to a pertinent aspect of Applicant's disclosure to which these claims are directed, at least one variable sized register is represented by plural register objects, where different register objects are provided respectively for each possible size of the variably sized register.

Applicants' method and system of generating an intermediate representation allows emulation of subject processors which use variable-sized registers and avoids conflict between different instructions operating on data of different widths by creating a set of registers objects in the IR for each variable-sized subject processor register, where each register object is dedicated to data of a given width. For example, one register object can be dedicated for each of the following widths of data: a byte, a word and a long word. As described in the paragraph bridging pages 22-23 of the present specification:

> If no conflict regarding instruction size arises within a particular Basic Block of subject processor instructions (i.e., if all of the instructions within that Basic Block are of the same bit width), the data contained in the appropriate abstract register can be accessed freely. If, however, a conflict does arise (i.e., instructions of different bit widths are stored/read from a given subject processor register), the correct data may be derived by combining the contents of two or more abstract registers in an appropriate way. An advantage of this scheme is that the Core is simplified since all operations on abstract registers are carried out on 32-bit items.

Thus, independent claim 1 recites that at least one variable sized register is represented by plural register objects, where different register objects are provided respectively for each possible size of the variably sized register. It is admitted on page 9 of the Office Action that Aho fails to teach or suggest representing a variable-sized register by plural register objects, where Davidson is relied upon by the Examiner as disclosing this feature. However, Davidson also

fails to disclose this feature of the Applicant's method. In particular, referring to the portion of Davidson cited in the Office Action (column 72, lines 22-25), Davidson refers to memory locations of variable sizes, **not variable sized registers**. This distinction is clearly visible in the examples described in column 74, lines 25-35 of Davidson, which describes the following:

RV (Register Value)
MV (Memory Value without indirection and without indexing)
MVIND (Memory Value with indirection but without indexing)
MV1 (Memory Value with byte context)
MV2 (Memory Value with word context)
MV4 (Memory Value with long context)
MV8 (Memory Value with quad context)
MV16 (Memory Value with octa context)

RV represents a register value having a single size in the Davidson disclosure, while the MV memory values are qualified with a 1, 2, 4, 8 or 16-byte size attribute suffix. As such, Davidson teaches the use of variable sized memory values but does not teach or suggest that at least one variable sized register is represented by plural register objects.

Independent claims 1, 8, 10 and 11 recite, inter alia, generating a plurality of register objects in an intermediate representation where at least one variable sized register is represented by plural register objects with one register object being provided for each possible size of the variable sized register. Again, neither Aho nor Davidson disclose or suggest such an intermediate representation generation method. Accordingly, combining those references fails to create even a prima facie case of obviousness. Accordingly, Applicants respectfully submit that the rejection of claims 1, 8, 10 and 11 and their respective dependent claims should be withdrawn.

By representing a variable sized register with plural register objects, a variable sized subject register can be represented by separately addressable subsets of the subject register. Each separately addressable subset of the subject register can potentially hold its own expression, where the subsets may potentially concurrently hold their own expressions (depending upon the sequence of updates to the subsets). This aspect of Applicant's method allows multiple partially redundant expressions to be concurrently attached to different subset register objects of a single abstract register representing a single subject register. Davidson fails to teach or suggest that

multiple overlapping temporary names (TN's) may be concurrently "live," and it is admitted in the Office Action that Aho fails to represent a variable sized register by plural register objects. Thus, this feature of Applicants' method in claims 1-11 is not taught or suggested by the prior art, and it is respectively submitted that the present claims are further patentable over the cited prior art for this reason. Newly submitted claims 12-20 further clarifies these distinguishing features, and early allowance of claims 1-20 is earnestly solicited.

Still further, Applicants respectfully submit that neither Aho nor Davidson disclose generating an intermediate representation that is rooted in register objects. In fact, referring to pages 558-559 cited by the Office Action, when Aho refers to the term "register," Aho is referring to a physical register implemented in the CPU that runs the code that Aho is compiling. Aho's description of allocating and assigning registers concerns physical registers, not register objects representing abstract registers in the intermediate representation. In contrast, the use of the term "register objects" in Applicants' claims reference expressions derived from the code being translated. There is no teaching or suggestion in Aho that register objects are actually formed in the intermediate representation, nor is the concept of an abstract register addressed in Aho. The Office Action refers to Fig. 9.18 in Aho in asserting that each of the t1, t2, t3, t4 are 'expression objects.' Applicants note that no register objects for holding variable values are taught or suggested in Aho's dag representation in Fig. 9.18.

According to the Examiner's assertion that each of the t1, t2, t3, t4 are 'expression objects,' none of these objects represent relationships between fixed values and variable values represented by the plurality of register objects, as recited in the claims of the present application. Applicants respectfully submit that neither Aho nor Davidson discloses generating an intermediate representation that is rooted in register objects as embodied in claims 1-11. Accordingly, Applicants respectfully submit that the Section 103 rejection of claims 1-11 should be separately be withdrawn for this reasoning and these claims allowed.

CLAIMS 2 , 8 AND 11

More specifically with reference to dependent claim 2 and independent claims 8 and 11, Applicants' method recites "that a write operation to a variably sized register is effected by writing to the register object corresponding to the appropriate size and maintaining a record of

which register objects contain valid data. As described above, by representing a variable sized register with plural register objects, a variable sized subject register can be represented by separately addressable subsets of the subject register. Each separately addressable subset of the subject register can potentially hold its own expression (potentially concurrently), which allows multiple partially redundant expressions to be concurrently attached to different subset register objects of a single abstract register representing a single subject register. Neither Aho nor Davidson teach or suggest multiple concurrent partially redundant overlapping register fields in the intermediate representation and, thus, do not effect the write operation to a variably sized register by writing to register objects of appropriate size and maintaining a record of which subsets of register objects contain concurrent valid data. Accordingly, Applicant respectfully submits that claim 2, 8 and 11 are separately patentable over the cited prior art and the Section 103 rejection of these claims should be withdrawn.

CLAIMS 3, 8 AND 11

Referring more specifically to dependent claim 3 and independent claims 8 and 11, this claim recites that a read operation from a variably sized register is effected by determining from the record maintained if there is valid data in more than one corresponding register object which must be combined to give the same effect as reading from the variable register. The Office Action cites the use of multiregister operations in Aho in rejecting claim 3. However, the multiregister teaching on page 565 of Aho describes operations which use two or more registers that are explicitly or implicitly addressable in the instruction set. Applicants' method described in claim 3 does not relate to operations addressable in multiple physical registers. To the contrary, according to claim 3, a single read access to a variably sized register is performed where the register is represented by separately addressable subset register objects. This single variably sized register is implemented by combining those expressions held in the subset register objects, where the exact method of combining the contents of the register objects depends on the most recent pattern of writes to those subset register objects as detailed in the record maintained in claim 2. The concept of the difference between subject processor registers and abstract registers (register objects) is of particular importance when considering the effect of variable-sized registers, as described on page 23, lines 7-21 of the subject application. The Aho disclosure concerns multiple physical registers. Neither Aho nor Davidson teaches or suggests

performing a read operation on a single variable sized register, where the read operation is effected by the data contained in the corresponding register objects. Accordingly, Applicant respectfully submits that dependent 3, 8 and 11 are separately patentable over the cited prior art and the Section 103 rejection of these claims should be withdrawn.

CLAIM 5

Paragraph 15 of the Office Action rejects claim 5 under U.S.C. § 103(a) as being obvious over Aho in view of Davidson and further in view of U.S. Patent No. 6,463,582 to Lethin. Applicants respectfully traverse this rejection and submits that the claims at issue are patentable over those patents for the following reasons.

Applicants' dependent claim 5 recites a method of dynamically translating program code according to the methods recited in the claims from which it depends therefrom. Applicants note that it is admitted in the Office Action that Aho fails to teach or suggest dynamically translating program code, where the Lethin patent is relied upon in the Office Action for teaching these features. As set forth above, the present application claims priority to GB Patent Application No. 9822075.9 and has an effective priority date of the October 10, 1998 filing date of GB Patent Application No. 9822075.9. It can be seen from the copy of the certified priority document submitted concurrently herewith that GB Patent Application No. 9822075.9 fully supports the claims in the present application. The Lethin patent was not filed until October 21, 1998, after the effective priority date of the present application. Thus, the Lethin patent is not prior art to the present application and all rejections in the Office Action relying upon the teachings the Lethin patent should be removed. Further, Applicants note that Davidson discloses what is known as a "static compiler." Such a compiler completely translates a particular program into another language before execution. The amount of time taken to perform such a translation is therefore relatively unimportant when compared to methods of dynamic translation such as that addressed by Applicants' claim 5. Accordingly, none of the cited prior art alone or in combination teaches or suggests Applicants' claimed method of dynamically translating program code, and Applicants respectfully submit that the rejection of claim 5 should be withdrawn.

CLAIM 9

Initially, Applicants assert that claim 9 is patentable over the cited prior art for the same reasons set forth above in distinguishing claim 1 over the prior art. Applicants submit the claim 9 is further separately patentable over the cited prior art in that neither Aho nor Davidson teaches or suggests the step of determining whether or not the contents of more than one abstract register must be combined and if so which abstract registers must be combined is determined in accordance of whether the data for each set of different sized abstract registers lies wholly within one valid abstract register or in more than one valid abstract register. As described in the paragraph linking pages 25-26 of the subject application, the use of separate abstract registers for each width of data allows data to be accessed easily when a subject processor code which uses a single width of data is being emulated. Applicants' method only requires a calculation to be made (i.e., the combination of data of different widths) on those infrequent occasions when data of different widths are written to and read from a subject processor.

Davidson is cited in the Office Action as disclosing the above-described feature of claim 9 through its disclosure of a "data access tuple." However, the cited portion of Davidson in col. 33 describes references to data contained in memory, not to the contents of more than one abstract register object in the full set or subset of register objects, as recited in claim 9. In fact, the portion of Davidson cited in the Office Action specifically excludes the possibility that a data access tuple could be classified as a register object of the claim 9. Davidson describes "a data access tuple is a tuple which causes a value to be loaded from or stored into memory ... the only difference between a register and a normal memory location of the CPU 25 is that the 'address' of a register can only be used in a data access tuple." By this very statement, Davidson itself clearly distinguishes memory locations from register contents, and Applicants respectfully submit that registers and normal memory locations are not equivalents.

Further, in column 7, lines 43-49, Davidson teaches the presence of a store tuple in the described example. These teachings of Davidson evidence that abstract registers are not used to reference tuples that define their contents, as recited in Applicants' method described in claim 9. A store tuple (or elsewhere, a "data access tuple") needs to be fully evaluated to return a result (e.g. the store tuple needs an address to be evaluated, since that address can be an expression

which returns different values on different executions). The abstract registers recited in Applicants' claim 9 directly point to expressions, so it can be seen that they are completely different from Davidson's data access or store tuples. Accordingly, Applicant respectfully submits that dependent 9 is separately patentable over the cited prior art and the Section 103 rejection of claim 9 should be withdrawn.

Conclusion

In view of the foregoing remarks and amendments, Applicants respectfully submit that the subject application is in condition for allowance. Applicants, therefore, respectfully request reconsideration and early notice of allowance.

Respectfully submitted,

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Dated: 2/24/05

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Amendments to the Drawings

In response to the objections to the drawings, Applicant has submitted herewith Replacement Sheets for Figs 5-7 to the drawings to eliminate the use of the numerals 1, 2 and 3 to designate intermediate representation blocks in Figures 6 and 7. In particular, the numerals 100, 200 and 300 have been respectively substituted for 1, 2 and 3 in Fig. 6. In Fig. 7, the numerals 100, 200a, 200b and 300 have been respectively substituted for the numerals 1, 2a, 2b and 3.